EasyChair Preprint

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Internally Generated Scan Resets Using OCC

Dan Jacobs and Vinod Naik

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ITC 2024: Internally generated scan resets using OCC.

Dan Jacobs Vinod Naik
Infineon Technologies. Lynnwood WA US

Abstract

This paper is about defining DfT architecture for generating internal scan reset pulse using OCC. Traditional approaches for providing scan reset can lead to certain limitations in the face of limited IOs, and limited ATE resources. Together these can cause coverage limitations, pattern inefficiency, or even unreliable patterns. So, to overcome these limitations, a DfT architecture is defined which generates scan reset internally using OCC.

1. Introduction

Traditionally for many chips, scan resets are driven from pads. But for designs with limited IOs this may not be feasible. Even if it is feasible, it certainly limits scan data bandwidth because of limited ATE resources.

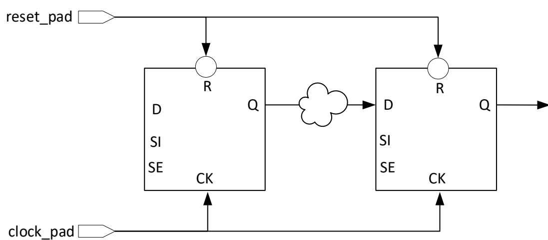


Fig 1-1, Pad is used to drive scan reset.

Alternatively scan enable can be used to enable or disable the reset during scan capture and scan shift respectively as shown in figure 1-2.

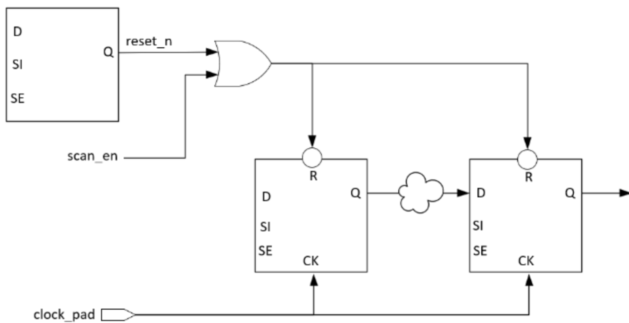


Fig 1-2, Scan Enable used to block reset_n during shift.

However, using scan enable to block both reset and retention controls create a race condition between retention control and async reset as shown in figure 1-3.

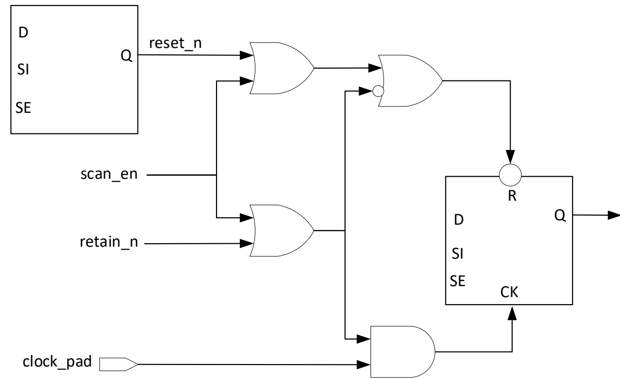
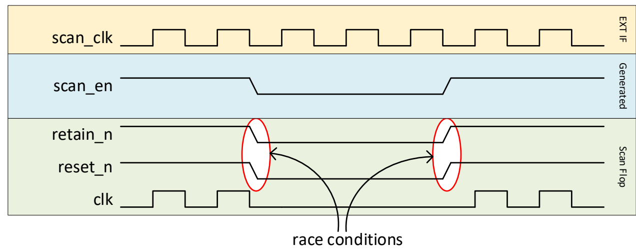


Fig 1-3, Scan Enable used to block reset_n and retain_n.



Waveform 1-1, The race conditions, if reset_n and retain_n events happening at same time.

2. Discussion

By using internal scan reset source, the pad which was reserved for driving scan reset can be used as another scan data pin thus maximizing scan data bandwidth. The scan clock pin can be used for both providing scan clock and internal scan reset with caveat of that the scan clock must be free running and cannot be distributed to any flops without an OCC.

As depicted in Fig 1-3, the scan enable used for scan reset control and retention control introduces race conditions so one way to avoid these race conditions is to use dedicated occ to generate reset pulse.

As depicted in Fig 2-1, reset_OCC is used to provide internal scan reset. This reset_OCC can be mini-OCC it requires only slow clock for its operation and required to generate only one pulse in capture window. The reset_OCC output is inverted and is gated with scan enable to block shift clocks going to reset pin of the scan flops. The reset_n signal shown in waveform 2-1 is output of reset_OCC.

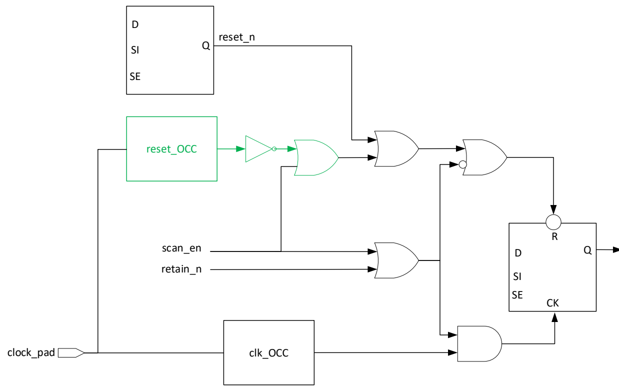
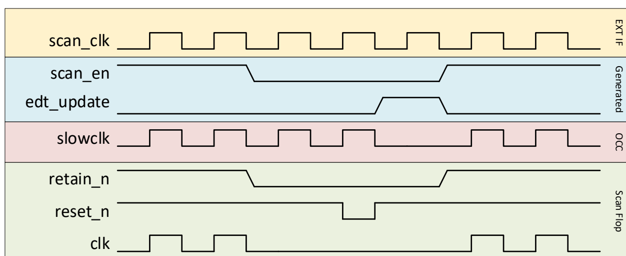


Fig 2-1, OCC used to provide internal scan reset.

As shown in Waveform 2-1, The reset events and the retention events are separated which resolves the race condition issue.



Waveform 2-1, Scan reset pulse and retention control at different time event in capture window.

Using OCC allows us to condition OCC at ATPG runtime according to the requirement. OCC is standard DFT instrumentation in DfT insertion Flow and by default having this OCC the clock is not pulsing when reset is pulsed and vice-versa.

The retention control must be deasserted in shift and can be asserted or deasserted in capture. One caveat is that retention control must not be allowed to be changed in capture window because of capture clock or scan resets.

The benefits of using this DfT architecture

- Leaves more IO bandwidth for Scan Data
- Provides retention flop coverage capabilities
- Provides scalable solution with minimal area impact such as localized hierarchical DfT
- Provides optimal coverage support for retention and asynchronous reset networks in same ATPG session
- Uses a standard DfT instrumentation
- Tool supported insertion and pattern generation flow

3. References

[1]https://docs.sw.siemens.com/en-US/doc/852852118/202309028.atpg_gd/id72df4fb2-4991-470c-ad44-e244c0cbdd37