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Review on Current and Future Prospective of FinFET Technology and It'S Challenges

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Review On Current and Future Aspects of FinFET Technology and It's Challenges

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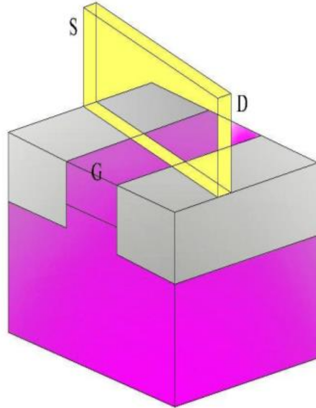
Abstract:

Transistor is a very big and most important research of all time in IC field industry. firstly, invented transistor was point contact transistor then shockley introduced improved version of transistor in 1948 and finally first commercial transistor came into effect in 1950, which was very big in size. As time passes customer requirement has been changed and main drawback was transistor's big size, so size starts reducing after BJT and FET, FinFET were introduced they were very small in size as compared to BJT and FET, but this reducing the size or scaling down the devices were introduced some other challenges. This review paper will briefly explain what are the current and future prospective of FinFET in IC technology and what are the challenges.

Key words: FinFET, short channel effect, DIBL, threshold voltage.

I. Introduction:

Moore's law states that "transistor density doubles in every 18 months"[1]. So, we have to scale down devices, scaling is nothing but a proportional adjustment of dimension of electronic devices while maintaining electronic properties of devices result in larger or smaller in size.
FinFET is basically an updated version of FET in which gate is placed in such a way gate form a fin like structure between source and drain. In 1990 it was first introduced to avoid short channel effect that generates from shrinking or scaling down of devices.
FinFET is designed in such a way that it will improve the short channel effect than MOSFET [2]
Conventional MOSFET used only for 65nm technology if device scaled down below this, MOSFET it's not possible to use this planner technology so we have to use multi gate or in FinFET technology to avoid short channel effect [3]. Firstly, Intel implemented finFET technology.



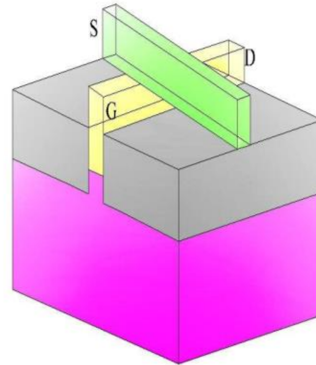


Figure-1(a) **Figure-1(b)**

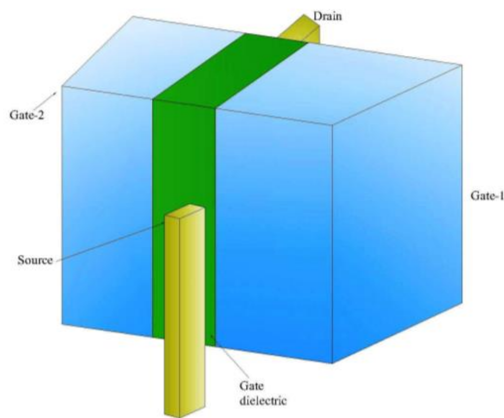
Figure 1(a) shows conventional MOSFET while Figure (b) shows FinFET device

Figure-1

II. Types of FinFet:

There are mainly two types of FinFET
1. Shorted gate FinFET (SG FinFET)
2. Isolated gate FinFET (IG FinFET)

In SG FinFET gates are physically shorted or connected so both get worked as one terminal does it is a three terminal device source, drain and gate.
In IG FinFET games are are physically isolated so both gates worked as terminal thus it is a four terminal device source, drain, gate 1and gate 2.



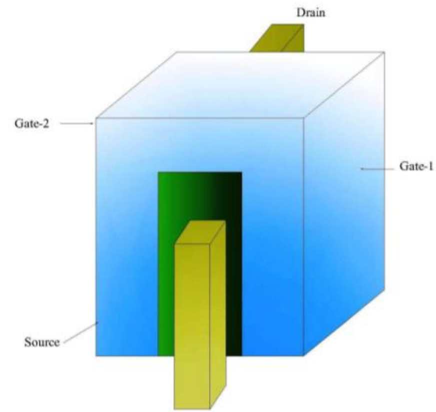


Figure 2(a) Figure 2(b)

Fig2(a) shows SG FinFET and fig 2(b) shows IG FinFET

III. **Optimization of short channel effect in FinFET** :

When we scale down the devices resulting all parameter will get affected but the most affected parameter are device length.

Due to scaling of Device minimum MOSFET device length decreases from 10 μm (in Mid 1970) to 1 μm range (in mid-1980).

Transistor channel length less than 3 to 5 μm system is called as short channel devices. The ratio between lateral and vertical dimension are reduced in short channel devices. Due to shrinking of devices channel length reduces and source and drain come closer to each other and gate loses its control over the device and leakage current starts flowing.

In electronic devices millions of transistors in a single chip, so overall power dissipation of devices becomes very high. short channel effect can degrade sub threshold slope and cause change in threshold voltage.

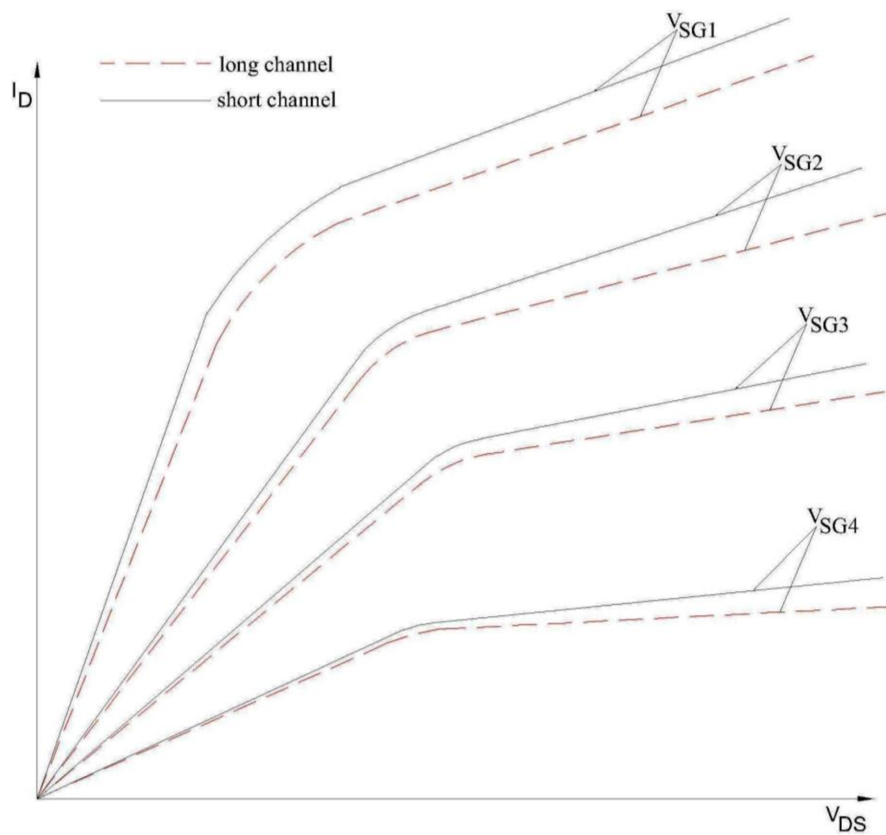


Figure-3

figure 3 shows a comparison between long channel Vgs (gate to source voltage) to short channel Vgs.

Here are main parameters which affects due to short channel length [5]

1. Drain introduced barrier lowering (DIBL)
2. punch through
3. velocity saturation
4. Surface scattering
5. Hot carrier effect
6. Hot electrons
7. Impact ionization

This paper emphasis about DIBL which is main challenges of reducing channel width. Conventional MOSFET gate has full control over device. If gate voltage is not applied and drain and source region are separated from each other than no drift current flows from drain to source only some diffusion current flows to higher concentration to lower concentration. A depletion region formed between highly doped source region and lightly doped substrate then junction becomes reverse bias. If gate voltage is applied electrons start depleting near surface, this voltage increased to threshold level and devices is on state. This is applicable for long channel devices.

Short channel devices source and drain comes very close to each other, so current starts flowing even without applying gate to source voltage, this effect has no control over the device is called as short channel effect (DIBL) [6].

FinFET is formed in 3D format effective length between drain and source increases so no current flows even when device is off mode. FinFET can easily minimize effect like short tunnel effect and drain induced barrier lowering even without heavy channel doping
Lightly doped or undoped channel have greater mobility so that it has low transverse electric field [7]. And this makes impurity scattering is very much low as you can consider it negligible it all makes FinFET have very small depletion and lower capacitance and sub threshold tends to reach 60mV/dec [8].
The short channel effect happens main lead to drift velocity of electron and off state leakage current. Due to scaling the of devices drift velocity and mobility of electron changes this leads to change in threshold voltage and this can be controlled by geometry i.e., to form fin. And for the off-state leakage silicon film should not be greater than quarter of channel length [9].

IV. **Future work and challenges:**

There is also width limitation and technology minimum witdh nowadays we are using is 5 nm and it is used by Intel. first generation 22nm process released in 2012 since then for 9 years technology is used it will continue to play an important role in next few years.But below 5nm FinFET is not reliable ,channel mobility decreases and again leakage becomes a big issue ,power dissipation of device increases so a new technology introduced.

Gate All Around FET(GAAFET) [10] which also nano wire transistor in which 5nm to 3nm technology used. GAAFET then a latest technology nano shit transistor is designed in which channel is surrounded by the gate to give better control than FinFET. Nano sheet technology is also called as Multi-Bridge Channel FET(MBCFET), it is latest technology available in market. MBCFET consumes low power and have high performance.

Complexity is also main challenge for these transistors; it is also very difficult to design and verify millions of transistors and to meet their market demand

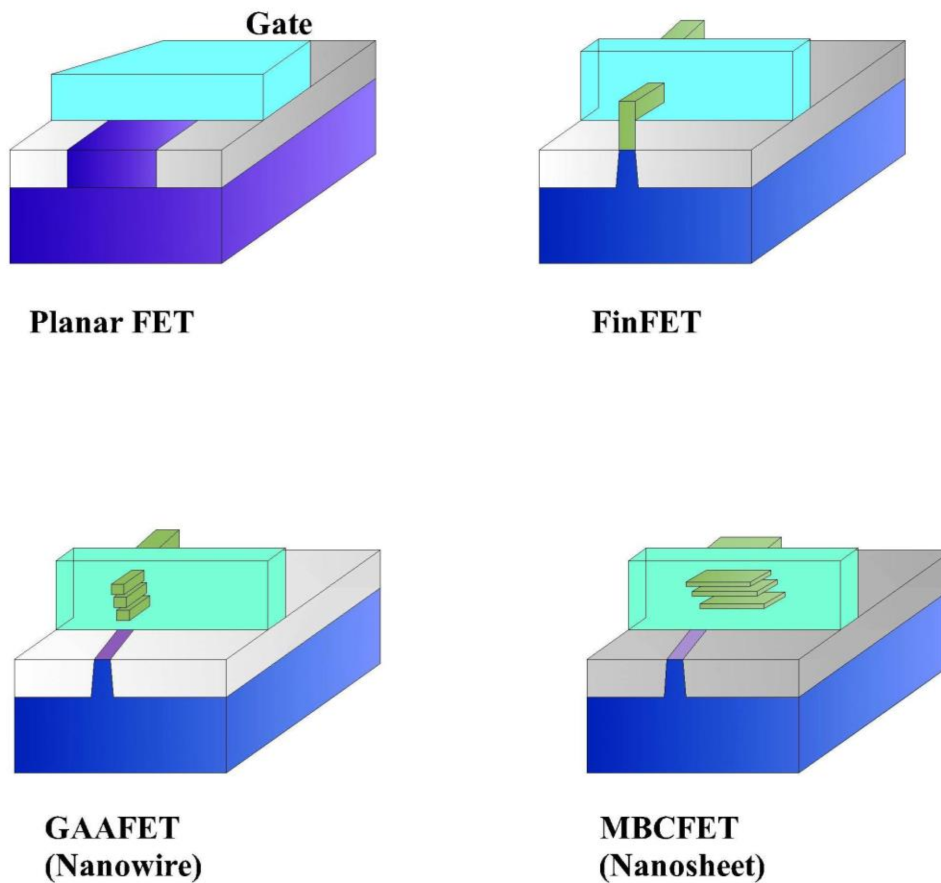


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Figure 4 shows systematic evaluation of transistor technology

V. Conclusion:

As a conclusion, FinFET is best alternative to solve challenges that happens in planer MOSFET beyond 22nm technology, and FinFET very much effective to avoid short channel effect. There is some limitation of it i.e., beyond 5nm technology it can't be used. FinFET have better controllability over the channel, it consumes lower power than MOSFET, have better switching speed and higher drain current means that is overcomes DIBL effect.

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