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A Novel Ultra-Low Voltage Fully Synthesizable Comparator Exploiting NAND Gates

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A Novel Ultra-Low Voltage Fully Synthesizable Comparator exploiting *NAND* Gates

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***Abstract*—In this work a novel ultra-low voltage, ultra-low power fully synthesizable comparator is presented. The proposed architecture exploits only 2-input *NAND* gates, that allow minimization of the area footprint and scalability up to extremely low supply voltages. An extensive simulation campaign in a 130 nm CMOS technology has shown state-of-the-art performance in terms of power-delay-product for supply voltages down to 0.3V. Simulations also show good robustness under mismatch and PVT variations, proving the feasibility of the approach.**

***Index Terms*—Dynamic comparator, fully-synthesizable, standard cell-based, ultra-low voltage, ultra-low power, Internet of Things.**

I. Introduction

In today's world, the Internet of Things has become ubiquitous, making our daily lives much easier through the use of smart devices. These devices enable us to effortlessly carry out routine tasks such as banking, booking, traveling, and more. Furthermore, with the advance of nano-technology, biomedical devices took hold in treating of nervous system disorder, paving the way to a novel field of application focused on ultra-low voltage (ULV) and ultra-low power (ULP) devices. Indeed ULV and ULP building blocks are preferred in many modern applications to increase the autonomy of devices, and to reduce the heating, promoting energy-harvested systems. In this regard, digital standard cells have been investigated as potential solutions to lower the minimum supply voltage into the deep sub-threshold range [1]. This approach can effectively decrease the human design effort needed and ultimately reduce costs. Several standard cell-based circuits have been proposed in literature as Operational Transconductance Amplifiers (OTAs) [2]–[5], comparators [6]–[10] filters [11], [12] and so on, showing the effectiveness of the standard cell approach in an ever constrained supply voltage range. In addition, even if standard cell-based architectures can work at supply voltage lower than 0.3V (e.g. also at 0.15 V [7]), it has to be noted that their performance over process, supply voltage and temperature (PVT) variations vary significantly with respect to nominal condition. Thus, they can be considered less robust with respect to their analog counterparts which, however, require an increasing design time and effort and can't reach ultra-low voltage performance exploiting conventional design strategies and architecture [4], [5].

Among the most useful building block in sensor interfaces, comparators stand out especially in analog-to-digital converters. Indeed, several digital-based comparators have been proposed in the recent literature, showing state-of-the-art performance in terms of power consumption as well as delay. In [13] a fully synthesizable comparator based on 3-input *NAND* gates (NAND-3) was proposed. However, the design has a limited input common mode voltage due to the use of *NAND* gates. Thus in [10] a comparator based on the same design but with a symmetric part based on NOR-3 gates was proposed. To optimize performance with respect to the input common mode voltage, a MUX was added to select either the NAND-3 or NOR-3 path. In [6], [7], a comparator that nested both the NAND-3 and NOR-3 paths was presented with the aim of achieving a rail-to-rail input common mode range. In contrast, [8] proposed a standard cell-based comparator using And-Or-Inverter (AOI) gates to enhance performance of [6], [7] with respect to power consumption (P_D). This work presented a novel ultra-low voltage, ultra-low power, and very fast comparator that uses only NAND-2 gates from the standard cell library, resulting in an aggressively optimized area consumption. Extensive simulations using 130 nm CMOS technology demonstrated state-of-the-art performance in terms of delay and also power-delay-product (PDP).

II. Proposed Architecture

The proposed architecture is depicted in Fig. 1 and is composed by eight *NAND-2* gates. The input signal is applied to the two instances $I_{0,1}$ of the comparator. Instances $I_{2,3,4,5}$ form the positive feedback which allows the architecture to be pre-charged in the negative clock phase, whereas in the positive clock phase it allows to regenerate the differential input signal due to the feedback loop.

In order to better understand the working principle of the proposed architecture the truth table of the *NAND* gate is recalled in Fig. 2. The *NAND* gate can be thought as a logic

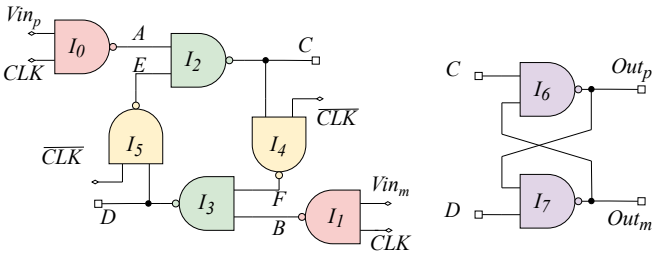
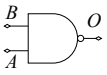


Fig. 1: Topology of the proposed comparator.



A	B	O
0	0	1
0	1	1
1	0	1
1	1	0

Enable	In	Out
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 2: Truth table of the *NAND* gate.

gate which has an enable signal: when the enable is low (i.e. GND), the output of the gate is pre-charged to 1 (i.e. V_{DD}) and is insensitive to other input signal variations, when the enable signal is high (i.e. V_{DD}), the gate behaves as an inverter for the other signal.

Taken in mind this, we can proceed with the description of the circuit. The analysis of the circuit can be divided in two phases:

1) CLK = 0: the $NAND$ gates $I_{0,1}$ are pre-charged to 1 (V_{DD}), thus $I_{2,3}$ behave as two inverters as well as gates $I_{5,4}$ which thus form a positive feedback which hold the data (see Fig. 3);
2) CLK = 1: the $NAND$ gates $I_{0,1}$ behave as two inverter which amplify the input signal $Vi_{p,m}$ to the input of $I_{2,3}$. Gates $I_{5,4}$ are disabled ($\overline{CLK} = 0$) and thus $I_{2,3}$ behave as two further inverters which amplify the input differential signal (see Fig. 4).

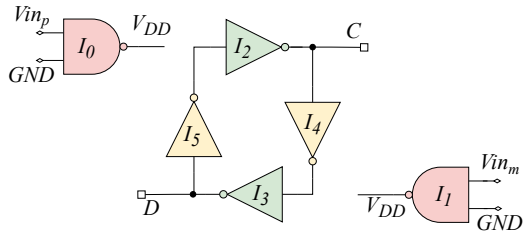


Fig. 3: Equivalent circuit under working condition when $CLK = GND$.

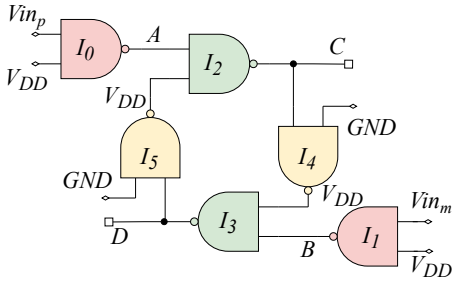


Fig. 4: Equivalent circuit under working condition when $CLK = V_{DD}$.

A $NAND$ latch composed by instances $I_{6,7}$ is used to hold the data when the CLK is low. The timing diagram of the proposed dynamic comparator is shown in Fig. 5.

With respect to the literature, the proposed architecture can operate with lower supply voltage. For a given supply voltage, a $NAND$-3 gate has more stacked devices (e.g [6], [7]), thus the drain source voltage of each device is lower. This results in a lower peack current, hence in a lower speed. Exploiting $NAND$-2 gates thus should result in an higher speed for the same supply voltage and, potentially, in a lower minimum supply voltage.

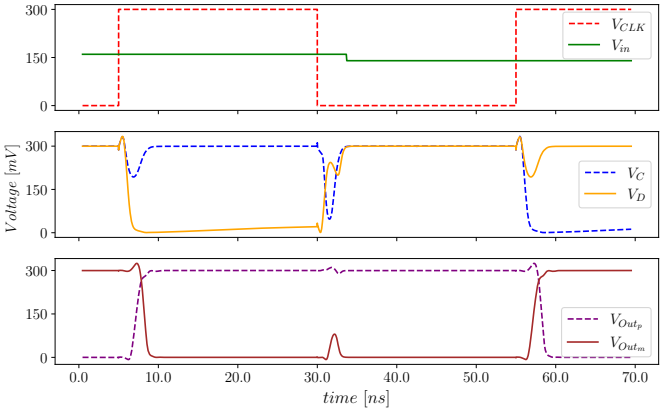


Fig. 5: Timing diagram of the proposed dynamic comparator during an evaluation phase.

III. Design and Simulation

The proposed architecture has been designed and validated on Cadence Environment in a 130nm ST-Microelectronics technology. Since the focus of the paper is to attain the lower power consumption we consider only minimum size standard cells.

In this way, the power consumption is minimized, the PDP performance is optimized and enhanced due to the effectiveness of the architecture which behaves in a lower voltage profile.

The architecture has been synthesized and tested by using the verilog netlist depicted in Fig. 6. In addition, from the netlist of Fig. 6 and through Cadence Innovus tools it has been extracted the automatic layout whose amount of Area is about 64.15 μm^2.

```
module COMPARATOR(
input Vinp,
input Vinm,
input CLK,
input CLKn,
output VOutp,
output Voutm
);

wire A,B,C,D,E,F;

NAND2_X2 I_0(
.I0(Vinp),
.I1(CLK),
.OUT(A)
);

NAND2_X2 I_1(
.I0(Vinm),
.I1(CLK),
.OUT(B)
);

NAND2_X2 I_2(
.I0(A),
.I1(E),
.OUT(C)
);

NAND2_X2 I_3(
.I0(F),
.I1(B),
.OUT(D)
);

NAND2_X2 I_4(
.I0(C),
.I1(CLKn),
.OUT(F)
);

NAND2_X2 I_5(
.I0(D),
.I1(CLKn),
.OUT(E)
);

NAND2_X2 I_6(
.I0(C),
.I1(VOutm),
.OUT(VOutp)
);

NAND2_X2 I_7(
.I0(D),
.I1(VOutp),
.OUT(VOutm)
);

endmodule
```

Fig. 6: Netlist of the comparator written in verilog.

In the following sections, main performance of the proposed comparator have been evaluated and robustness with respect to PVT and mismatch variations has been assessed.

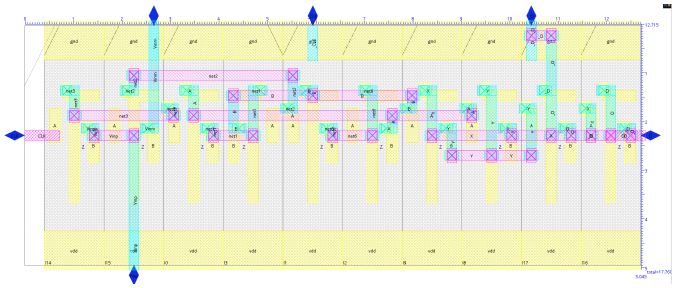


Fig. 7: Layout generated from netlist of Fig. 6 through Cadence Innovus tool: the total amount of Area is about 64.15 μm^2 (5.045μm x 12.715μm).

A. Power consumption and delay of the Comparator

The power consumption and the delay of the comparator have been tested with considering different power supply voltages: $V_{DD} = [0.3, 0.6, 0.9, 1.2]$ $[V]$, with an input differential voltage of 10 mV, an input common mode voltage equal to $V_{DD}/2$ and a sampling frequency of 10 Hz accordingly to [6], [7]. Results of the analysis have been depicted in Tab. I. As it can be observed, the power consumption is very low, especially in 0.3V and 0.6V cases. In the 0.3V case the power consumption is as low as 23 nW. For what concerns the delay it decreases with the increasing of the supply voltage and thus with the increasing of the power consumption. The PDP is maximized at 0.3V, with a nominal value of about 0.148 fJ. In addition, the Energy Delay Product (EDP) has been computed also considering different clock frequencies according to the scaled performance of the four different supply voltages. Results show that a minimum value of 0.008 fJ/MHz is attained at $V_{DD} = 0.6V$, whereas a maximum frequency of 1GHz can be reached at $V_{DD} = 1.2V$.

TABLE I: Power consumption and Delay of the proposed comparator under different supply voltages, with considering an input common mode voltage of $V_{DD}/2$ and an input differential voltage of 10 mV.

V_{DD} $[V]$	0.3	0.6	0.9	1.2	0.3	0.6	0.9	1.2
f_{clk} $[Hz]$	10				20M	200M	500M	1G
Delay [ns]	6.56	0.61	0.290	0.201	6.56	0.61	0.736	0.201
P_D [μW]	0.023	0.931	9.32	39.95	0.064	2.66	24.77	79.61
PDP [f J]	0.148	0.567	2.71	8.01	0.422	1.616	9.34	16
EDP [fJ/MHz]	14.8k	56.77k	271k	801k	21.1m	8.08m	18.7m	16.0m

B. Offset of the proposed comparator

In this Section the offset of the comparator under different power supply voltages has been characterized in typical condition and also versus mismatch variations. In Tab. II the nominal offset voltage of the comparator and the mean value and standard deviation of the histograms depicted in Fig. 8 have been reported. In Tab. II the result of 200 montecarlo mismatch-only simulations have been summarized. As it can be observed, the offset mean value (μ) and standard deviation (σ) increase with lower supply voltage. When the constraints over the supply voltage are relaxed, the comparator reaches lower offset voltage with lower σ_{off} (they have to be normalized with respect to the power supply voltage). However, since the offset is related also to the size of transistors, it can be decreased accordingly to the Pelgrom law [14], by increasing the size of instances $I_{0,1,2,3}$ which mainly contribute to the offset voltage.

TABLE II: Offset of the proposed comparator over different supply voltage in typical condition and under mismatch variations.

	V_{DD} $[V]$	0.3	0.6	0.9	1.2
Typical	$[mV]$	10	5	-2	-1.2
Mismatch	$\mu[mV]$	1.3	5.25	1.55	0.51
	$\sigma[mV]$	22.85	21.88	11.71	14.32

C. Performance vs Process and Temperature Variations

In this section performance versus process and temperature variations have been analyzed. In Tab. III performance over 200 montecarlo process-only variations have been summarized for different supply voltage. As it can be observed, the mean values are in good agreement with those reported in Tab. I. For what concerns temperature variations, we reported in Tab. IV the performance when temperature of 0 and 80 degrees have been reached. As it can be observed, at each supply voltage the power consumption is lower at 0 deg, and that is due to the threshold voltage dependence of standard cell transistors with respect to the temperature.

IV. Comparison

In this section a comparison against the literature has been presented and depicted in Tab. V. As it can be observed, with respect to the literature the proposed work can perform with very low supply voltage and only [7] can work with lower supply voltage. For what concerns the delay, the proposed architecture reaches the best delay in all the supply voltage range, reaching at 1.2 V a delay of 201 ps. Also at 0.3V the proposed comparator reaches the lower delay, which amount to about 6.56 ns. For what concerns the power consumption, the minimum power consumption is reached by [7] at 0.15 V of supply voltage. In order, to better evaluate the trade-of between Power Consumption and Delay, the PDP has been reported and, as it can be observed, the proposed architecture reaches the minimum PDP with respect to the recent literature. With respect to the offset voltage, the proposed architecture is in line with the literature whereas the minimum offset voltage is reached by [8].

V. Conclusion

In this work a novel type of fully synthesizable comparator that operates at ultra-low voltage levels has been presented. To validate the comparator's performance, Cadence simulations were carried out using a 130nm ST-Microlectronics technology. The results of the analysis show that the proposed comparator is highly robust with respect to process, voltage, and temperature variations. Additionally, the comparator was found to be faster than other state-of-the-art comparators in the literature and produced a lower PDP. Overall, these findings suggest that the proposed comparator is a promising candidate for low-power, high-performance applications.

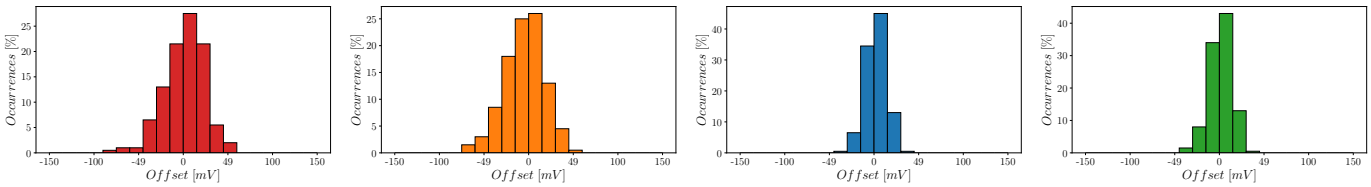


Fig. 8: Histogram over 200 Montecarlo mismatch only iterations of the offset voltage of the proposed comparator when supply voltage is equal to 300 mV (red), 600mV (orange), 900 mV (blue) and 1.2V (green).

TABLE III: Power consumption and Delay of the proposed comparator under process variations for different supply voltage, with considering an input common mode voltage of $V_{DD}/2$, a clock frequency of 10 Hz and an input differential voltage of 10 mV.

V_{DD} $[V]$	0.3		0.6		0.9		1.2	
	μ	σ	μ	σ	μ	σ	μ	σ
Delay [ns]	6.540	1.315	0.615	0.070	0.287	0.024	0.203	0.010
Power Consumption [μW]	0.021	0.005	0.918	0.166	9.311	1.084	39.873	4.595
PDP [f J]	0.137	0.021	0.565	0.098	2.672	0.271	8.094	0.863

TABLE IV: Power consumption and Delay of the proposed comparator under temperature variations for different supply voltage, with considering an input common mode voltage of $V_{DD}/2$, a clock frequency of 10 Hz and an input differential voltage of 10 mV.

V_{DD} $[V]$	0.3		0.6		0.9		1.2	
T [deg]	0	80	0	80	0	80	0	80
Delay [ns]	10.04	3.88	0.667	0.57	0.36	0.44	0.186	0.236
Power Consumption [μW]	0.01	0.074	0.665	1.57	12.68	19.12	37.52	47.74
PDP [f J]	0.108	0.29	0.443	0.89	4.55	8.35	6.98	11.27

TABLE V: Comparison with the literature

	This Work				[7]			[8]			[13]
Technology [nm]	130				180			45			40
V_{DD} [V]	1.2	0.9	0.6	0.3	0.6	0.3	**0.15**	1	0.6	0.35	0.6
Delay [ns]	**0.201**	0.290	0.61	6.56	740	34.7k	442k	1	68	2.1k	2
Power Consumption [μW]	39.95	9.32	0.931	0.023	1.95m	0.024m	**0.006m**	6.29	9.23m	0.244m	0.5
PDP [fJ]	8.01	2.71	0.567	**0.148**	1.9	1.0	3.5	6.3	0.63	0.51	1
σ_{off} [mV]	14.32	11.71	21.88	22.85	23	8	31	5.78	5.81	**4.73**	40

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