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AN EVALUATED OPTIMAL DESIGN OF FULL ADDER AND FULL SUBTRACTOR IN QUANTUM-DOT CELLULAR AUTOMATA

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Abstract.A newly emerging Quantum-dot cellular automata technology seems to be very attractive nowadays for research purposes because it follows various specifications like high packaging density and speedy. It has fast switching frequency and can be scaled preciously with less power requirement. In this paper, we design a QCA circuit. This paper proposed the novel design of a full adder and a full subtractor which has the least number of cell count. The output is shown with the QCA Designer tool and then the result is compared with the result of previous papers presenting full adder and subtractor.

Keywords: QCA, adder and subtractor, least cell design, least possible area.

1. Introduction

Nowadays CMOS technology lags, as it has faced various disadvantages like it absorbs high noise ,consumes more power and it shows effect of short circuit, and reduced gate control. So it is quite difficult to further create VLSI circuits with CMOS technology which will able to consumes less power and give high speed as well as density. After CMOS, QCA is new upcoming technology. In QCA technology polarisation of electrons represents digital information. QCA allows very high operating frequencies that can be in tetra hertz range. Its integratable device density is also very high which is more than 900 times that of current CMOS scaling limits. It also have potential to reach upto very fast speed and ultra-low power consumption. It is above mentioned unbelievable characteristics develops research craze for it in researchers mind. The heart of every processor's arithmetic unit is an adder. It is most important in all operations because all other operations like subtraction, division, and multiplication can be implemented by using adders. So for designing a good arithmetic circuit we have to put our focus on making an efficient adder circuit.

In this paper we tried to put more work on the best possible least cell design of adder as well as subtractor that present in paper [28], we found that if we decrease the particular three cells in each design our output we get as desired. This decreases cells and because of decreasing cells area is also seems to decrease.

This paper is structured as follows: The detailed background of QCA technology is presented in section 2. In section 3 the design is proposed with simulation result. The Section 4 presents the result with the comparison table of the

various previous design. The conclusion is given in section 5. Section 6 shows all helpful references.

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2. Background of QCA Technology

If we compare QCA technology with a classical computer, so there we see the difference as in QCA the representation of digital information is in the form of electrons pair arrangement that forms quantum dot arrays. Every cell in QCA is generally made from four-electron sites that generally called quantum dots . There is a tunnel junction that couples these four electrons sites. In the cell there exist two moving electrons. By tunnelling, we mean that the moving electron can occupy freely any quantum sites inside cell. With coulomb interactions which are generally found between alternate cells, there is seen information transfer.

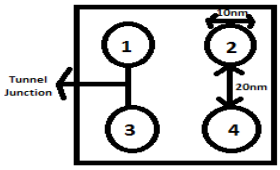

Figure 1: Basic QCA cell

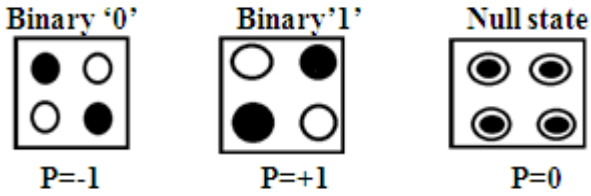

Figure 2: The encoded binary Information of polarized QCA

Because of electrostatic or magnetic fields, there can be seen the adjacent cells interacts to each other and the occurrence of state changes. The below figure represents four quantum dots in quantum dot cellular automata. The cell polarization are represent by two states of polarizations that is -1 for binary 0 and +1 for binary 1.

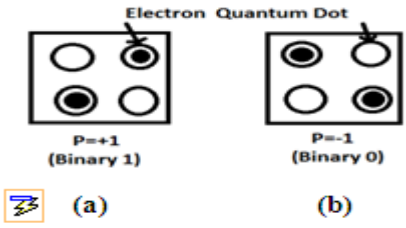

Figure 3: Four quantum dots in quantum dot cellular automata
(a) P= +1 (Binary 1), (b) P= -1(Binary 0).

The above figure represents a square shaped space inside which it has two free electrons that form a quantum cell. In the square, there is a hole in every corner

generally called as quantum dots. Because of Coulomb interaction, electron pair move inside each cell and then the cell polarity is determined by the position of electrons in the cell. As we know that the polarization has two values +1 and -1, that depends on the electron's position, which can also be termed as binary logic one and zero

In QCA the application of wire is similar to that of the wire used in the real world. Wire is nothing but a side by side connection of QCA cells that propagates a binary signal from one end of input to the other end that is till output. Regular cells and rotated cells are two types of generally used cells from which wire is constructed. These two types of cells are shown in the figure below as follows.

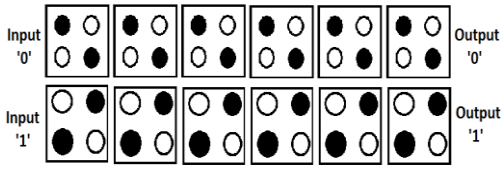

Figure 4: QCA wire(90 degrees)

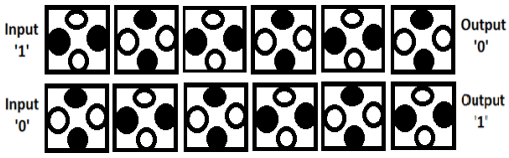

Figure 5: QCA wire (45 degrees)

Information that flows inside every circuit is generally controlled by the clock. This clock provides the power to run the circuit. It provides true power gain of the circuit. Cells are only powered by the clock and apart from it, there is not at all any other external source. Polarization of input cell can be fixed and then as a concluded outcome the system seems to relax to the ground state. This whole relaxation process involves certain steps which are shown below as follows.

- Release: Between the tunnel junction there seems a potential barrier, the less the potential barrier is, it becomes easier for the electron to excavate from one dot to another.
- Relax: When it is found the potential barrier is at the lowest possible state.The polarization of cell in this condition is said to be '0'. All previous input state of the cell removes this relax stage.
- Switch: Switch position is a position in which new input is given and then the potential barrier is increased automatically with state of the input cell, the QCA cell gets polarised easily. In this state, the certain estimation of the QCA occurs.
- Hold: Now the potential barrier is heightened as possible. And thus now it is easily possible to suppress any future electron tunnelling, so after a point, it seems the state is fixed

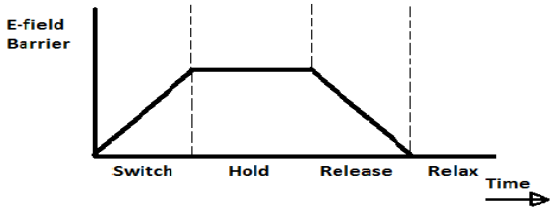

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Figure 6: Four phases of a clock.

In QCA, one of the logic gates plays a very important role in designing purpose it is called majority voter abbreviated as MV. It has five cells in which three of them are input cells whereas another one is used as an output cell, and a center cell, is used as a decision-making cell.

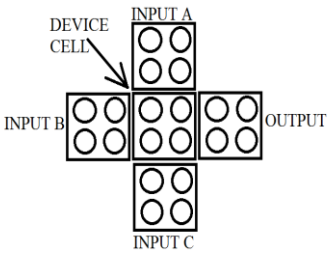


Figure 7: Majority voter (MV) gate in QCA

A	B	C	OUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

AND Logic
When one input is set to "0"

OR Logic
When one input is set to "1"

Figure 8: Truth table of majority voter gate.

3PROPOSED DESIGN WITH ITS SIMULATION RESULT.

The QCA design of full adder and subtractor are presented in the QCA Designer simulation tool. QCA Designer simulation tool is used to stimulate computational logic circuit constructed using QCA. It can be very simple to construct complex Quantum Dot cellular Circuits using this very simple tool. The engines are used for simulation that is Bistable simulation engine & the Coherence Vector Simulation Engine that is used by the tool.

3.1 Full Adder

The Adders are used to performs the Number's addition. Each one bit inputs A,B,C are added using one-bit full-adder. We get two outputs at the end, one of the output is called SUM and another one is called Carry The full adder block diagram with its truth table are shown below.

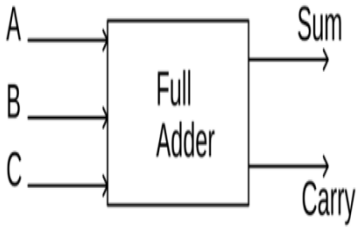
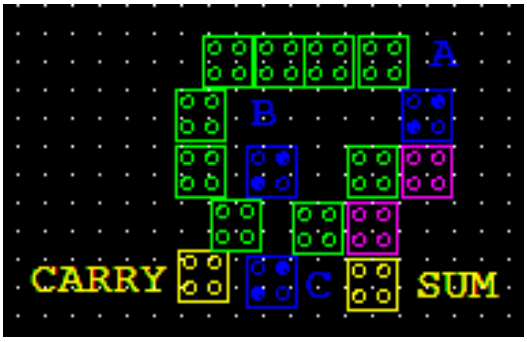


Figure 9: Block diagram of full adder.

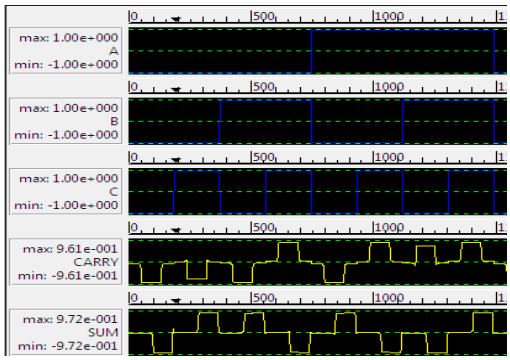
Input			Output	
A	B	C	Sum = S	Carry = C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 10: Truth table of full adder.

The below figure shows the proposed Full-Adder circuit using the QCA designer tool.



(a)



(b)

Figure 11 :(a) full adder circuit in QCA, (b) its simulation result.

In this proposed design, of the Adder requires just 16 QCA cells with only two clock cycle. The required area for this design is 0.012 μm^2.

3.2 Full subtractor

Subtractor is used to subtract one number from another. Full subtractor performs subtraction between two binarybit. Here we take three input naming as input A, input B, and input C. We get the difference and borrow bit as output. The full subtractor block diagram with its truth table is shown in the figure below:

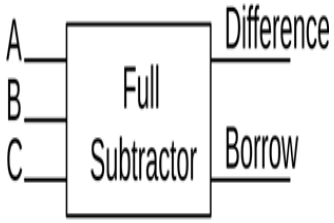
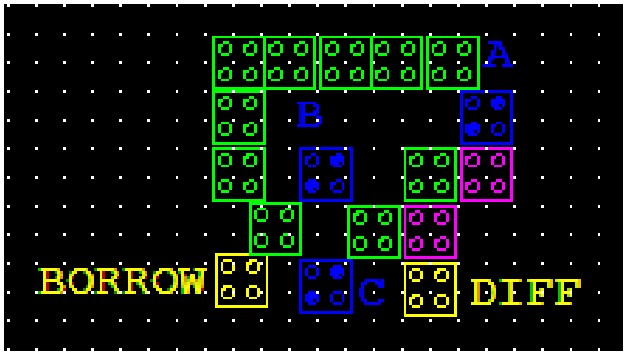


Figure 12: Block diagram of full subtractor

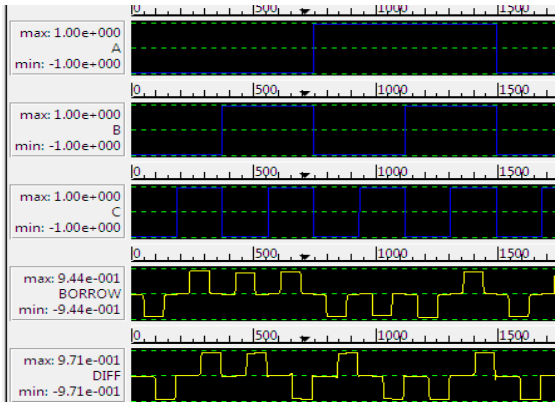
Input			Output	
A	B	C	Difference = D	Borrow = B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Figure 13: Truth-table of full subtractor

The below figure shows the proposed Full subtractor circuit using the QCA designer tool with its simulation result



(a)



(b)

Figure 14: (a)full subtractor QCA circuit,(b) its simulation result.

The full subtractor proposed here includes 17 cells and occupies an area of about 0.012 μm^2. Here, the two clock phases are used to generated the proposed design.

4 COMPARISION

Various papers are compared and the comparison table is shown below as follows. The proposed design presented in this paper required the least possible cells and thus shows a reduction in area and low power consumption. And thus be found best designs for the application.

Comparison table of QCA Full adder circuit

S.NO	REFERENCE	CELL COUNT	AREA
1	REF[1]	198	0.206
2	REF[2]	168	0.228
3	REF[3]	154	0.180
4	REF[4]	135	0.144
5	REF[5]	124	0.097
6	REF[6]	107	0.920
7	REF[7]	105	0.146
8	REF[8]	96	0.120
9	REF[9]	95	0.087
10	REF[10]	93	0.086
11	REF[11]	79	0.050
12	REF[12]	73	0.044
13	REF[13]	71	0.060

14	REF[14]	69	0.070
15	REF[15]	63	0.050
16	REF[16]	61	0.030
17	REF[17]	59	0.043
18	REF[18]	52	0.038
19	REF[19]	51	0.034
20	REF[20]	44	0.060
21	REF[21]	41	0.030
22	REF[22]	38	0.020
23	REF[23]	33	0.020
24	REF[24]	31	0.019
25	REF[25]	30	0.011
26	REF[26]	29	0.020
27	REF[27]	23	0.010
28	REF[28]	19	0.014
29	**PROPOSED DESIGN**	16	0.012

Figure 16: Comparision table of QCA Full adder circuit

Comparison table of QCA Full Subtractor circuit

S.NO	REFERENCE	CELL COUNT	AREA
1	REF[29]	186	0.206
2	REF[3]	154	0.180
3	REF[30]	136	0.168
4	REF[31]	108	0.120
5	REF[32]	104	0.028
6	REF[33]	84	0.027
7	REF[34]	63	0.050
8	REF[35]	53	0.047
9	REF[36]	46	0.015
10	REF[37]	37	0.040
11	REF[38]	32	0.028
12	REF[39]	27	0.030
13	REF[28]	20	0.014
14	**PROPOSED DESIGN**	17	0.012

Figure 17: Comparision table of QCA Full subtractor circuit

The adder, subtractor circuit proposed design presented in this paper requires less cell count and due to a decrease in cells in shows a reduction in area. And thus found a good design for the application.

5. CONCLUSION

At the Nanoscale circuit design level, QCA is the new emerging technology. QCA seems to be very realiable for the design of complex logic circuits and low-power-consuming logic circuits. The theoretical basis of Quantum Cellular Automata is discussed in this relevant QCA background for the research purpose. The basic elements of this technology like wire and clock are explained here. The above-explained design shows adder and subtractor QCA circuits with least QCA cells that minimizes size. This paper presents improved design of adder and subtractor and then implemented using QCA designer tool which shows its better performance compared to all previous design. Various papers are compared and then the best over the best design of adder and subtractor with the least number of cells used are shown in this paper. This design required the least possible area.

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