EasyChair Preprint

№ 5317

An Embedding Circuits Design on Marriage Problem Predicate in Making Integrated Circuit

Frank Appiah

June 9, 2021

AN EMBEDDING CIRCUITS DESIGN ON MARRIAGE PROBLEM PREDICATE IN MAKING INTEGRATED CIRCUIT.

Frank Appiah

Abstract—This is about embedding circuits on the digital circuits on Marriage Problem Predicate to define a digital integrated circuit(ic). The making of integrated circuit is described in this article with schematic capture of circuits. A complete setup of IO connections is made in the process of defining the connection entries. Finally, this research demonstrates an example of IC called MarriageIC.

Index Terms—digital circuit, logic circuit, design, simulation, ic, truth table, timing diagrams.

• *Frank Appiah is with King's College London, King's Engineer Group, UK. E-mail: appiahnsiahfrank@gmail.com*

1 Introduction

The following are used in forming binary set on tabular representation :
MbA={0, 1, 0, 0, 0}.
MbX={0, 0, 0, 1, 1}.
MbS={0, 0, 1, 0, 0}.
MbR={1, 0, 0, 0, 0}
MbW={0, 1, 0, 0, 0}.
MbNg={0, 0, 0, 1, 1}.

Tabular Representations On Binary Set

Table 1.

B	MbA	MbNg	MbR	MbW	MbX	MbS
N1	0	0	1	0	0	0
N2	1	0	0	1	0	0
N3	0	0	0	0	0	1
N4	0	1	0	0	1	0
N5	0	1	0	0	1	0

Truth Table 2

MbA	MbW	And	Or	Xor
0	0	0	0	0
1	1	1	1	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0

The Digital logic((MbA, MbR)=(and,or,xor)) ={(0,0)=(0,0,0), (1,1)=(1,1,0)}

For example Digital set (MbA, MbX) will show the following :

Digital set (MbA, MbX)={(0,0), (0,0), (0,0), (0,1), (0,1)}.

The binary logic will now be operator treated on the above Digital set.

Truth Table 3

MbA	MbX	And	Or	Xor
0	0	0	0	0
1	0	0	1	1
0	0	0	0	0
0	1	0	1	1
0	1	0	1	1

The Digital logic((MbA, MbR)=(and,or,xor)) ={(0,0)=(0,0,0), (1,0)=(0,1,1),(0,1)=(0,1,1)}

For example Digital set (MbA, MbS) will show the following :

Digital set (MbA, MbS)={(0,0), (0,0), (0,1), (0,0), (0,0)}.

The binary logic will now be operator treated on the above Digital set.

2 LOGIC CIRCUITS DESIGN

The design of logic circuit was done with Logic Circuit Sim Professional. This is the full version. It starts by creating a project with the tool. Here, I am actually using an Android mobile version. Two projects are created as shown below:

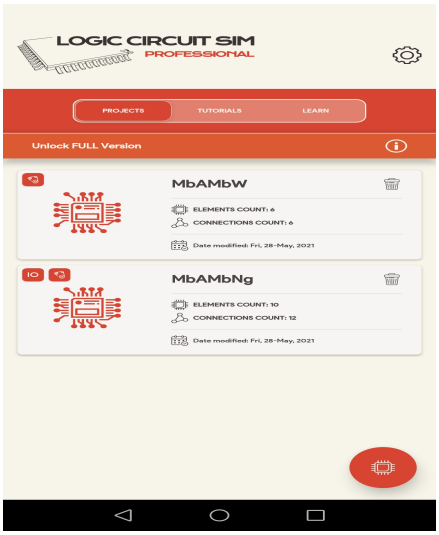


Figure 1

In the pictorials, you will see the number of logic elements, number of connections and date of modifications. The project names are MbAMbNg and MbAMbW.

I will describe the design of MbAMbW circuit[7] that has same name as the project. The variables are MbA and MbW.

Logic Function :
(1) *MbA.MbW*
(2)*MbA+MbW*

This is deduced from table 2.

Circuit Design of MbAMbW

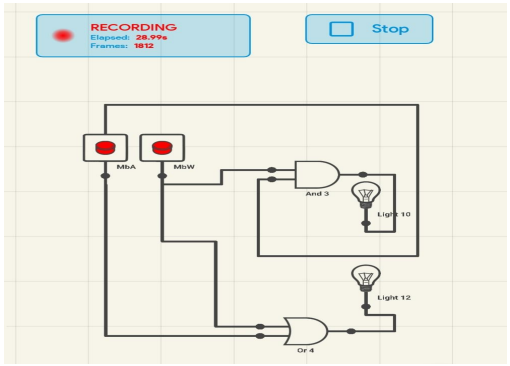


Figure 2

Timing Diagram of MbAMbW

Timing is done by recording the entry connections entered by selecting the points.
This in particular has 1.47 minutes of recording activity with the off/on Switch.

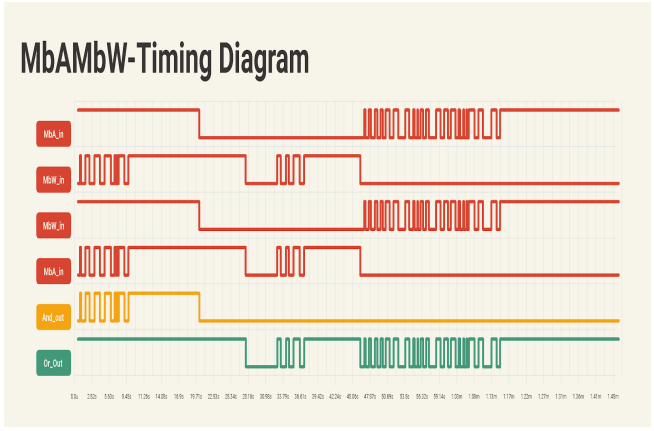
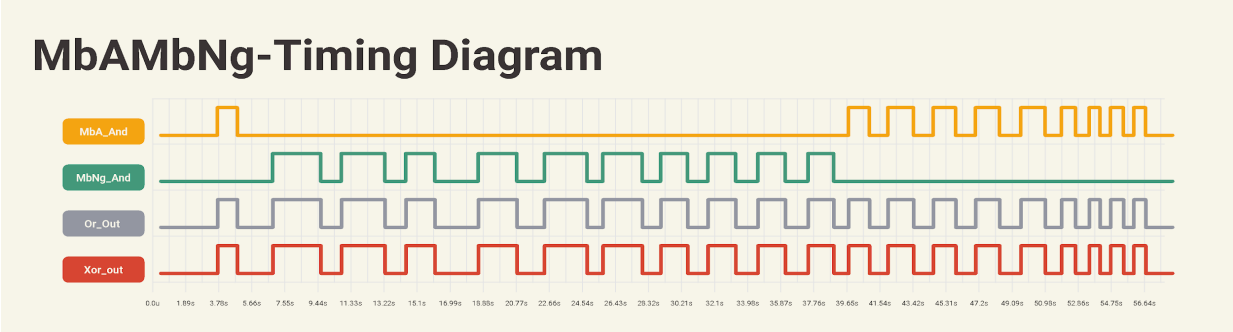


Figure 3

The above diagram is for each entry connection selected.



The and function has timing diagram And_out. The or function has timing diagram, or_Out.

The next is based on table 3

With variables MbA and MbNg,

The logic functions are:

(1) $\overline{MbA}.\ MbNg + MbA.\overline{MbNg}$

(2) $MbA.\ \overline{MbNg} + \overline{MbA}.MbNg$

CIRCUIT Design of MbAMbNg

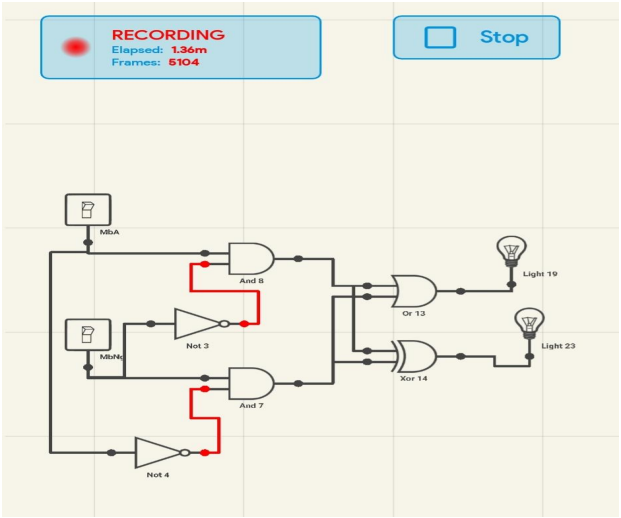


Figure 5

Timing Diagram on MbAMbNg. Figure 4.

The connection points are labelled as MbA_And and MbNg_And. Or_Out and Xor_out are both outputs.

3 INTEGRATED CIRCUIT DESIGN

In setting up an IC for MbANbW logic gate circuit, I will be using Logic Circuit Sim Professional (full version) in achieving this. The setup is as shown below :

Figure 6.

After pressing the setup button, the setup IO circuit screen shows up as shown below in the schematic capture :

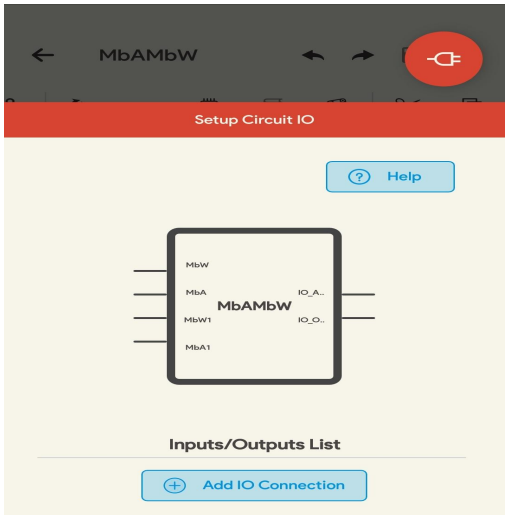


Figure 7.

Then you click the Add I/O Connection button which will show the "Please select Io node" screen with single selection mode activation. The following labelled IO points

are in orange color in the preview after :

1.MbA
2.MbNg
3.IO_or
4.IO_Xor

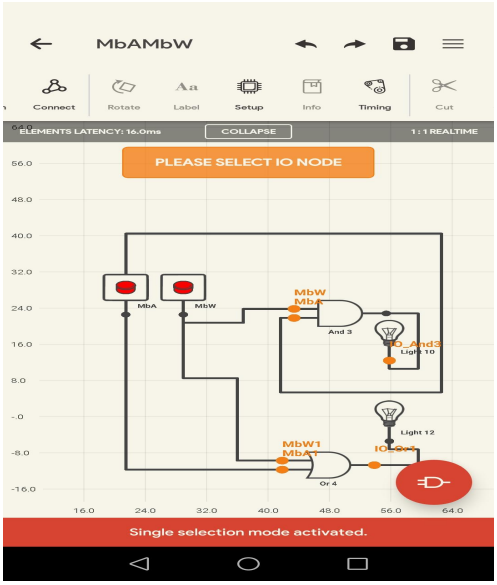


Figure 8.

The input /output list for I/O Connection added will as shown below in the schematic capture :

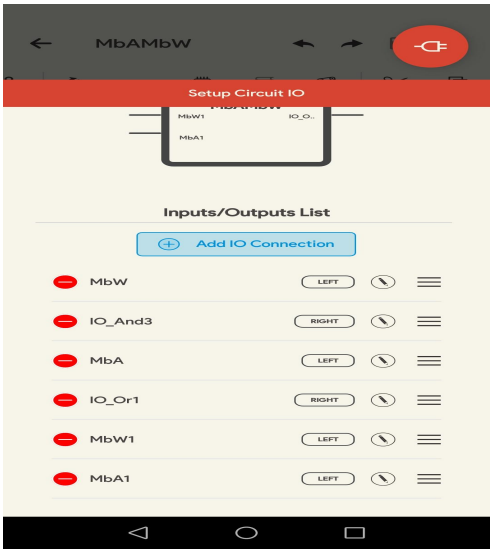


Figure 9.

The next setup for MbAMbNg logic circuit is shown in the steps below in the schematic captures:

1.

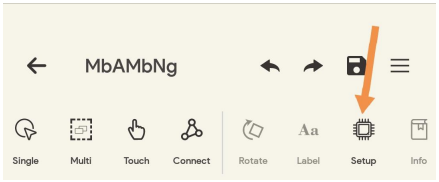
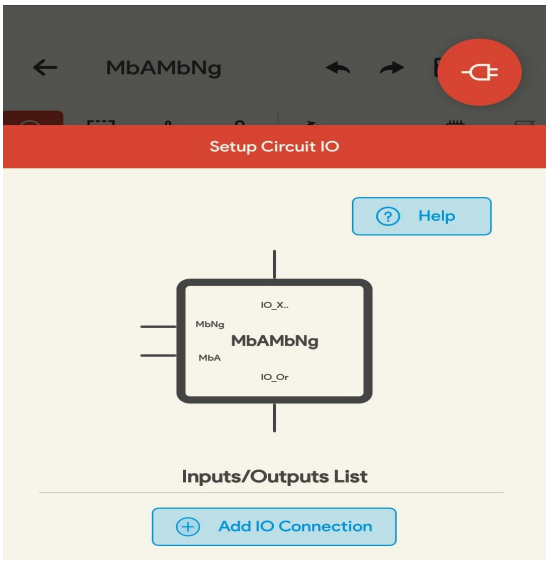
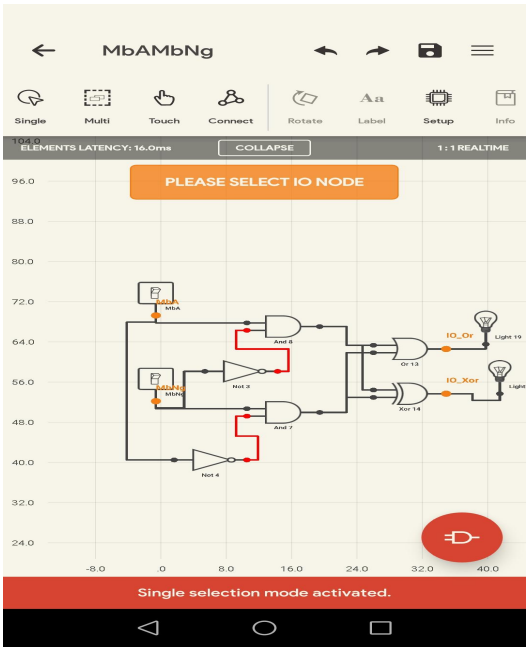


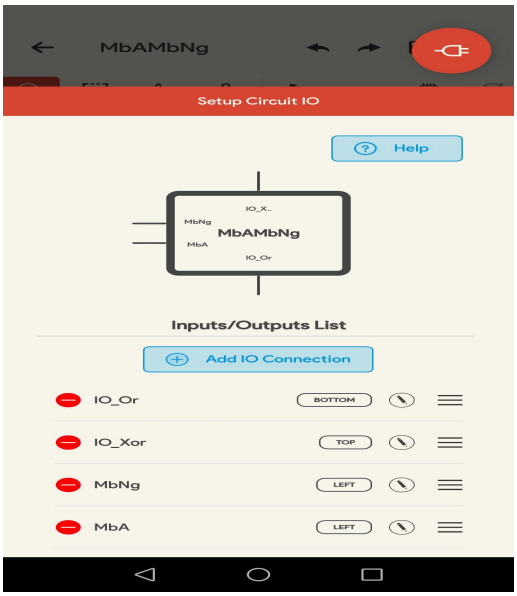
Figure 10

2.

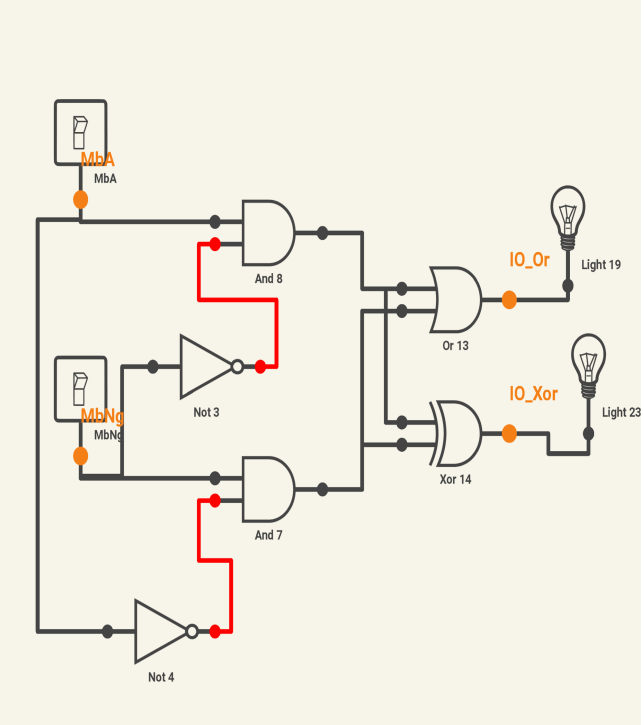


3.





4. Figure 14.

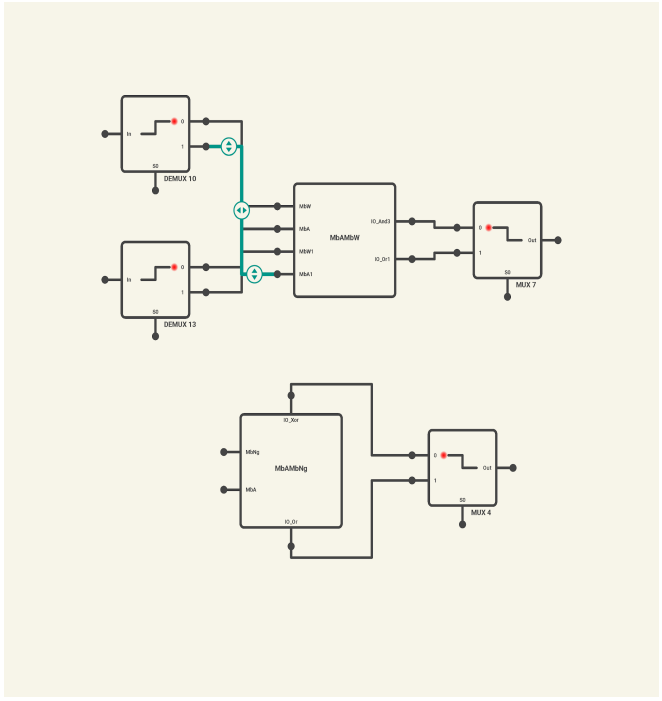


5.

The next stage is to show the completed ic elements in use. I start a new project then add the elements from the ic menu. The menu shows the ic elements of MbAMbW and MbAMbNg logic circuits.
To use is by just selecting them and these appears in the grid layout. These are as shown below in the schematic capture :

There are two inputs and two outputs for each embedded circuit/integrated circuit. A demultiplexer is placed in connection to each input to enable selection of one input at a time. For example, MbA and MbA1 inputs to select which is which, a select signal s will enable MbA if s=0 and enable MbA1 if s=1.

The circuit indication for that as described is shown below in the schematic capture :
Figure 16.



The rest of selection for input connections are shown also below in the schematic captures
:

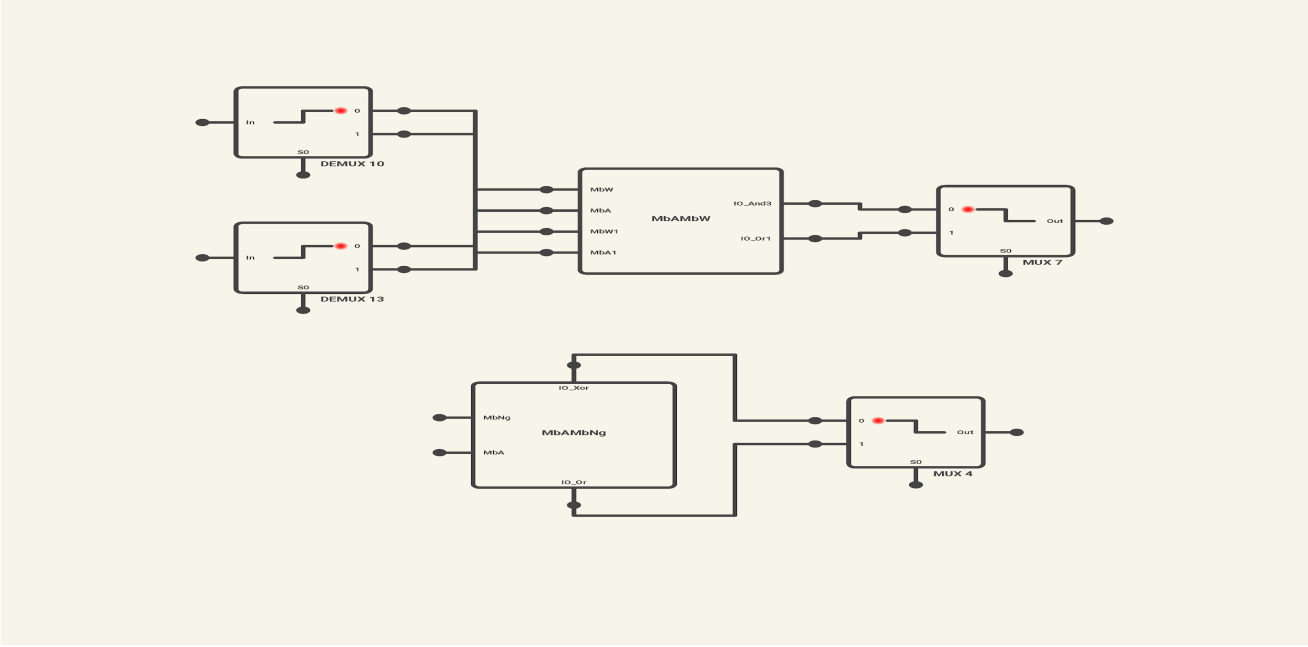


Figure 15.

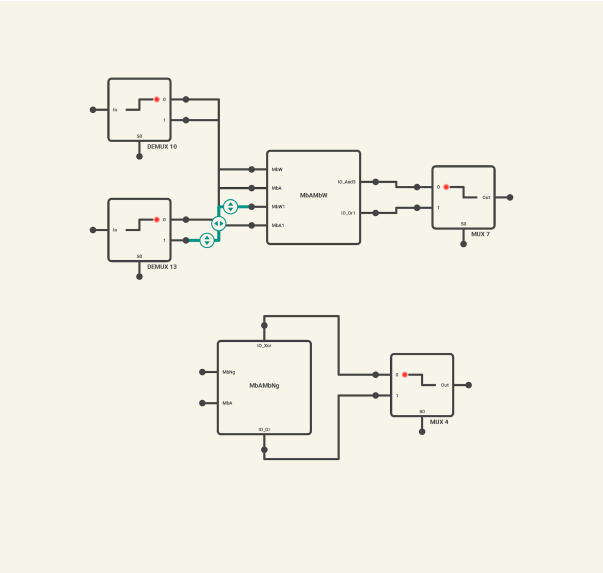


Figure 17

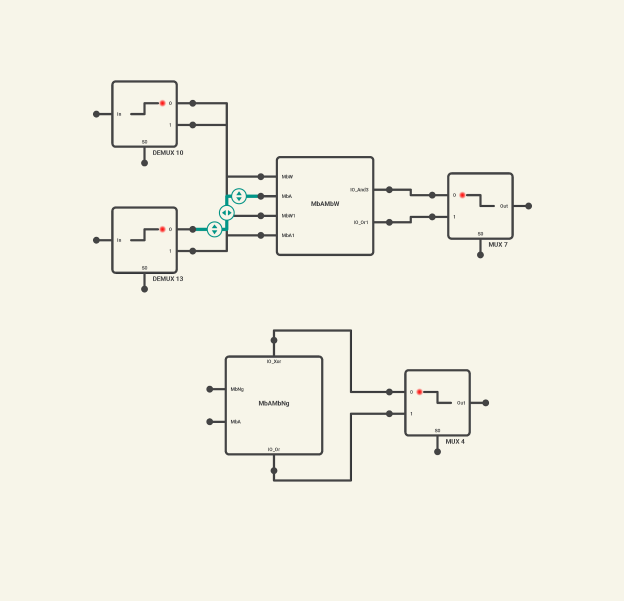


Figure 18.

On the output connection is also a multiplexer to select one output at a time. For MbAMbW ic, the outputs are IO_And3 which is selected when s=0 and IO_or1 when s=1 from MUX 7 multiplexer.
For MbAMbW ic, the outputs are IO_Xor when s=0 from MUX 4 multiplexer and IO_or when s=1 against MUX 4.

The two integrated circuit blocks are separated but MbA input can get the two connected into a complete circuit. This is shown in the schematic capture Figure 20:

A further connection will be necessary to create a more compact integrated circuit just like a physical chip package.

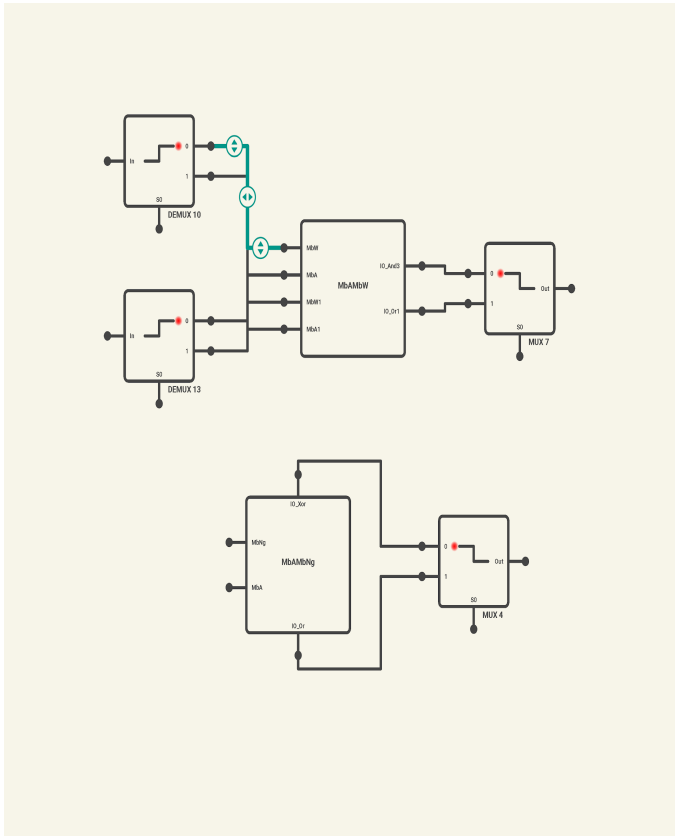


Figure 19.

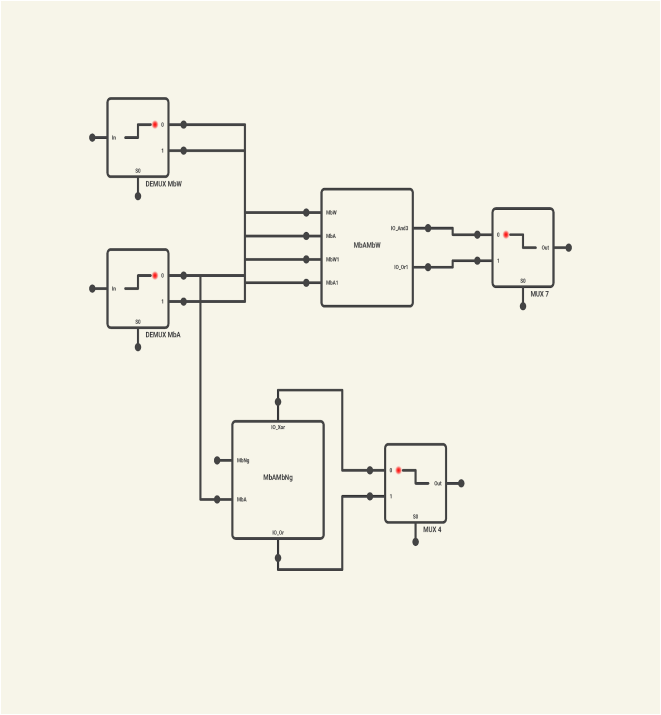


Figure 20.

This is as shown in the schematic capture :

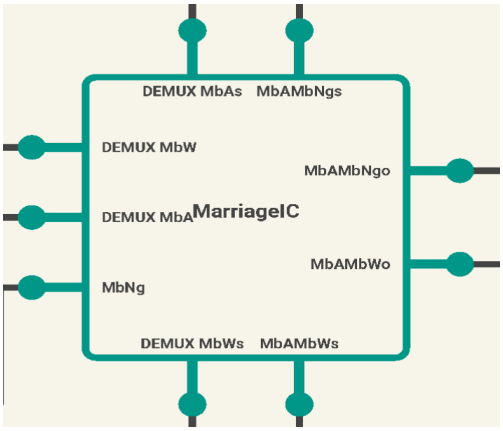


Figure 21.

4 FIGURES

3.1 Appendices

```
Figure 1        Figure 8
Figure 2.       Figure 9
Figure 3.       Figure 10
Figure 4.       Figure 11
Figure 5.       Figure 12
Figure 6.       Figure 13
Figure 7.       Figure 14 to 21.
```

5 CONCLUSION

This research looks mainly at essential logic circuit design based on predicate task involving a Marriage Problem [2,3,7]. The logic circuits are embedded to make integrated circuits.[9,10] Finally, a view on MarriageIC.

REFERENCES

[1] Vingron, S. P. (2012). Logic circuit design: Selected methods. Springer Science & Business Media.
[2] Appiah Frank. Letter Combinatorics : Theory on counting problems. EPSRC UK TuringAI Letter. 2020
[3] Appiah Frank. Letter Combinatorics : Theory on counting problems. Marriage Problem. Mendeley Publication. 2020
[4] Fisler, K. (1999). Timing diagrams: Formalization and algorithmic verification. Journal of Logic, Language and Information, 8(3), 323-361.
[5] Appiah, F. (2021). Digital Logic on Marriage Problem Predicate Task (No. 5317). EasyChair.
[6] Gates, S. C. (2004). Gate Design.
[7] Appiah, F. (2021). A Logic Circuit Simulation on Marriage Problem Predicate with Timing Diagrams. EasyChair Preprint no. 5317, version history
[8] Levi, I., & Fish, A. (2021). DUAL MODEL LOGIC: A New Paradigm for Digital Ic Design. Springer Nature.
[9] Geiger, R. L., Allen, P. E., & Strader, N. R. (1990). VLSI design techniques for analog and digital circuits.
[10] Claasen, T. A. (2003). System on a chip: Changing ic design today and in the future. IEEE micro, 23(3), 20-26.

Dr. Frank Appiah. He is a holder of Bsc(Hon) from Kwame Nkrumah University of Science and Technology in 2018, Msc in Advanced Software Engineering from King's college London in 2010 and PhD in computer science and engineering from both KCL (2012/2014) and KNUST (2014) respectively. Frank Appiah has professional certificates in Management and engineering since 2011 from IEEE. He developed StreamEPS - Stream Event Processing System in 2011 which is hosted at Github.